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EXPEDITED PROCEDURE - EXAMINING GROUP 2822

S/N 09/256,643 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Michael Trinh
Serial No.:	09/256,643	Group Art Unit: 2822
Filed:	February 23, 1999	Docket: 303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE	

RESPONSE UNDER 37 C.F.R. § 1.116

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In response to the Final Office Action dated 11 March 2002 and the Advisory Action dated 10 June 2002, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 21, 23, 24, 26, 29-33 and 36-75 are pending in the application. Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are rejected, and claims 33, 47, 62, 67, 70, and 75 are objected to. None of the claims have been amended.

Allowable Subject Matter

The Final Office Action indicated that claims 33, 47, 62, 67, 70, and 75 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 33, 47, 62, 67, 70, and 75 in independent form, but believes that the base claims from which they depend are allowable in view of the remarks made herein.

Rejections Under 35 USC § 103

Claims 21, 23-26, 29-32, 36-46, and 48-59 were rejected under 35 USC § 103(a) as being unpatentable over Chamberlain (U.S. Patent No. 4,473,836) taken with Halvis et al. (U.S. Patent No. 5,369,040, Halvis). The applicant respectfully traverses.

The remarks made in response to this rejection filed by the applicant on 21 November 2001 and 8 May 2002 are referred to and incorporated herein, and the following remarks are also made in response to this rejection.

Claim 43 recites a method of fabricating a transistor comprising, among other elements, forming a source region and a drain region in a substrate, forming an insulating layer on the substrate, forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0, and removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

Chamberlain discloses a photodetector structure shown in Figure 2 including a silicon substrate 11 having a diffused photosensitive region D1 that functions as a source and a diffused region D2 that functions as a drain. Chamberlain, column 3, lines 10-15. Chamberlain is deficient as a reference in that, as the Office Action stated, Chamberlain does not disclose forming a gate from a silicon carbide compound $Si_{1-x}C_x$ as recited in claim 43.

Halvis discloses a MOS photodetector with closely-spaced gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon. However, Halvis does not disclose forming a source region and a drain region in a substrate and forming an insulating layer on the substrate as recited in claim 43.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. The suggestion or motivation to combine references must be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). The motivation must also be "clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

The Final Office Action dated 11 March 2002 added the polysilicon and carbon gate of Halvis to the substrate of Chamberlain as the basis of the rejection under §103. The Advisory Action stated that the motivation for this combination was language in Halvis relating to the need for photodetectors with "improved quantum efficiency" and "improved response" and "improved performance" and "improved sensitivity." Halvis, column 1, line 64 to column 2, line 17. This language is very general and non-specific about the goals for new types of photodetectors, but does not provide a specific motivation for the technical combination made in the Final Office Action. This language from Halvis is not technically relevant to the specific combination of the polysilicon and carbon gate of Halvis with the substrate of Chamberlain. The Final Office

Action did not state how this combination would result in a photodetector with "improved performance."

In re Dembiczak requires that the motivation for the combination be "clear and particular." The language from Halvis referred to in the Advisory Action does not provide a clear or particular motivation for combining Halvis and Chamberlain. The Advisory Action further states that "Halvis expressly teaches to replace the polysilicon gate [of Chamberlain] with the polysilicon carbide gate." The Advisory Action did not identify such express language in Halvis. The applicant respectfully submits that there is no clear and particular evidence of a suggestion in the record for the combination of Chamberlain and Halvis.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-26, 29-32, 36-46, and 48-59 has **not** been established in the Final Office Action, and that claims 21, 23-26, 29-32, 36-46, and 48-59 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,449,941, Yamazaki) in view of Halvis. The applicant respectfully traverses.

The remarks made in response to this rejection filed by the applicant on 21 November 2001 and 8 May 2002 are referred to and incorporated herein, and the following remarks are also made in response to this rejection.

As stated above, the MPEP and case law require that there be some suggestion or motivation to combine references to reject claims under 35 USC § 103, and the suggestion or motivation must be found in the prior art. *In re Dembiczak* requires that the motivation be "clear and particular."

The Final Office Action stated in text bridging pages 3 and 4 that it would have been obvious "to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide .... taught by Halvis .... because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity." This language is not relevant to the specific technical combination of Yamazaki and Halvis, and is not clear and particular as is

required by *In re Dembiczak*. The applicant respectfully submits that there is no clear and particular evidence of a suggestion in the record for the combination of Yamazaki and Halvis.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 has **not** been established in the Final Office Action, and that claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Halvis taken with Tohyama (U.S. Patent No. 5,858,811) and Chamberlain. The applicant respectfully traverses.

The remarks made in response to this rejection filed by the applicant on 21 November 2001 and 8 May 2002 are referred to and incorporated herein, and the following remarks are also made in response to this rejection.

As stated above, the MPEP and case law require that there be some suggestion or motivation to combine references to reject claims under 35 USC § 103, and the suggestion or motivation must be found in the prior art. *In re Dembiczak* requires that the motivation be "clear and particular." As stated above, the Final Office Action and the Advisory Action did not provide a clear or particular motivation for combining Halvis and Chamberlain.

The Final Office Action also stated on page 5 that it would have been obvious "to remove portions of the insulating layer and the layer of silicon carbide of Halvis in forming the gate as taught by Tohyama, wherein forming diffused regions ... is taught by Chamberlain .... because of the desirability to control the desired thickness of the gate insulating layer..."

The Final Office Action did not cite prior art in the record that supports the above-stated motivations for combining Chamberlain, Halvis, and Tohyama. The applicant respectfully submits that there is no clear and particular evidence of a suggestion in the record for the combination of Chamberlain, Halvis, and Tohyama.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 has **not** been established in the Final Office Action, and that claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6973

Date 11 July 2002 By _____
Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 11th day of July, 2002.

Name Amy Moriarty Signature _____